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;PALASM Design Description

;---------------------------------- Declaration Segment ------------
TITLE    5. Versuch Teil a
PATTERN
REVISION
AUTHOR   ???
COMPANY  RWTH
DATE     06/24/02

CHIP  _versuch5  PALCE16V8

;---------------------------------- PIN Declarations ---------------
PIN  2          DA;
PIN  3          DB;
PIN  4          DC;
PIN  5          DD;
PIN  10         GND;
PIN  12         A                                       COMBINATORIAL ;
PIN  13         B                                       COMBINATORIAL ;
PIN  14         C                                       COMBINATORIAL ;
PIN  15         D                                       COMBINATORIAL ;
PIN  16         E                                       COMBINATORIAL ;
PIN  17         F                                       COMBINATORIAL ;
PIN  18         G                                       COMBINATORIAL ;
PIN  20         Vcc;

;---------------------------------- Boolean Equation Segment ------
EQUATIONS
A = (DA * /DB * /DC * /DD) + (/DA * /DB * DC * /DD);
B = (DA * /DB * DC * /DD) + (/DA * DB * DC * /DD);
C = (/DA * DB * /DC * /DD);
D = (DA * /DB * /DC * /DD) + (/DA * /DB * DC * /DD) + (DA * DB * DC * /DD);
E = (DA * /DB * /DC * /DD) + (DA * DB * /DC * /DD) + (/DA * /DB * DC * /DD) +
(DA * /DB * DC * /DD) + (DA * DB * DC * /DD) + (DA * /DB * /DC * DD);
F = (DA * /DB * /DC * /DD) + (/DA * DB * /DC * /DD) + (DA * DB * /DC * /DD) +
(DA * DB * DC * /DD);
G = (/DA * /DB * /DC * /DD) + (DA * /DB * /DC * /DD) + (DA * DB * DC * /DD);

;---------------------------------- Simulation Segment ------------
SIMULATION
SETF /DA /DB /DC /DD
CHECK /A /B /C /D /E /F G
SETF DA /DB /DC /DD
CHECK A /B /C D E F G
SETF /DA DB /DC /DD
CHECK /A /B C /D /E F /G
SETF DA DB /DC /DD
CHECK /A /B /C /D E F /G
SETF /DA /DB DC /DD
CHECK A /B /C D E /F /G
SETF DA /DB DC /DD
CHECK /A B /C /D E /F /G
SETF /DA DB DC /DD
CHECK /A B /C /D /E /F /G
SETF DA DB DC /DD
CHECK /A /B /C D E F G
SETF /DA /DB /DC DD
CHECK /A /B /C /D /E /F /G
SETF DA /DB /DC DD
CHECK /A /B /C /D E /F /G
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;PALASM Design Description

;---------------------------------- Declaration Segment ------------
TITLE    Veruch5 - Teil b
PATTERN
REVISION
AUTHOR   ???
COMPANY  RWTH
DATE     06/24/02

CHIP  _teilb  PALCE16V8

;---------------------------------- PIN Declarations ---------------
PIN  1          clk                                          ;
PIN  2          DA                                           ;
PIN  3          DB                                           ;
PIN  4          DC                                           ;
PIN  5          DD                                           ;
PIN  6          ENP                                          ;
PIN  8          LOAD                                         ;
PIN  10         GND                                          ;
PIN  11         OE                                           ;
PIN  12         QA                                REGISTERED ;
PIN  13         QB                                REGISTERED ;
PIN  14         QC                                REGISTERED ;
PIN  15         QD                                REGISTERED ;
PIN  16         RCO                               COMBINATORIAL;          ;
PIN  20         Vcc                                          ;

;---------------------------------- Boolean Equation Segment ------
EQUATIONS
RCO = (ENP * QA * /QB * /QC * QD * LOAD);

QA = (ENP * /QA * LOAD) + (/ENP * QA * LOAD);

QB = (ENP * QA * /QB * /QC * /QD * LOAD) + (ENP * /QA * QB * /QC * /QD * LOAD)
   + (ENP * QA * /QB * QC * /QD * LOAD) + (ENP * /QA * QB * QC * /QD * LOAD)
   + (/ENP * /QA * QB * /QC * /QD * LOAD) + (/ENP * QA * QB * /QC * /QD * LOAD)
   + (/ENP * /QA * QB * QC * /QD * LOAD) + (/ENP * QA * QB * QC * /QD * LOAD);

QC = (ENP * QA * QB * /QC * /QD * LOAD) + (ENP * /QA * /QB * QC * /QD * LOAD)
+ (ENP * QA * /QB * QC * /QD * LOAD) + (ENP * /QA * QB * QC * /QD * LOAD) +
(/ENP * /QA * /QB * QC * /QD * LOAD) + (/ENP * QA * /QB * QC * /QD * LOAD) +
(/ENP * /QA * QB * QC * /QD * LOAD) + (/ENP * QA * QB * QC * /QD * LOAD);

QD = (ENP * QA * QB * QC * /QD * LOAD) + (ENP * /QA * /QB * /QC * QD * LOAD) +
(/ENP * /QA * /QB * /QC * QD * LOAD) + (/ENP * QA * /QB * /QC * QD * LOAD);


;---------------------------------- Simulation Segment ------------
SIMULATION
SETF /LOAD /DA /DB /DC /DD /ENP /OE
clockf clk
SETF ENP LOAD
for i:= 1 to 10 do
begin
clockf clk
end

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